4.6 A Delay-Line-Based GFSK Demodulator for Low-IF Receivers

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There is a growing interest in low-power and low-cost wireless transceivers such as wireless PANs and sensor networks. Frequency shift keying (FSK) is a preferable modulation scheme because it requires less stringent linearity requirement on the power amplifier of the transmitter, and therefore is suitable for low-power architectures [1]. Gaussian filter is typically employed to generate Gaussian-FSK (GFSK) signal to limit the transmitted signal bandwidth and increase the number of channels. On the receiver side, a low-IF architecture is very popular due to high level of integration, low flicker noise, and no DC-offset problem. To recover the data from a GFSK-modulated IF signal, a demodulator is required in the receiver. Digital GFSK demodulators can provide digital detection but require variable gain amplifiers and ADCs, demanding high power consumption. Many analog or mixed-signal GFSK demodulators have been reported to reduce hardware complexity and power, but their chip size, power dissipation, and required signal-to-noise ratio (SNR) are still high [2]-[4]. In this work, a GFSK demodulator using a delay-line self-sampler and digital signal processing circuits is proposed to provide robust demodulation with low power consumption and a small chip area.

Shown in Fig. 4.6.1, the RF front-end and complex channel-select filter (CSF) are used to downconvert the RF signal to IF, reject the image, and select the desired channel. The limiter amplifies the IF signal to rail-to-rail swing to remove the AM noise and retain the frequency information. The proposed GFSK demodulator is shown inside the dashed box of Fig. 4.6.1. The time-to-digital converter (TDC), consisting of an analog delay line, DFFs and an encoder, converts the limiter output signal into digital codes. Rather than using an accurate high-frequency oversampling clock to perform TDC function [5], IF signal is sampled by its own delayed signal. The advantage of this technique is that the delay-line self-sampler can avoid edge synchronization problem and reduce power consumption. The IF in this work is chosen to be 5MHz to allow the TDC to generate sufficient frequency information for 1Mb/s and 250kb/s data detection. A moving-average (MA) circuit is used to improve the sensitivity. The threshold-generation (THG) circuit detects the peak and valley based on the output of the MA and optimizes the decision threshold for the slicer. Additionally, it can track and cancel the time-varying DC offset caused by frequency offset and frequency drift between the transmitter and the receiver. To remove the glitch of the raw data, a post integrate-and-dump filter (IDF) is used at the output of the slicer. Finally, a clock and data recovery (CDR) generates the corresponding 1MHz/250kHz clock and retimes the recovered output data.

Figure 4.6.2 shows the operating principle of the TDC based on the delay-line self-sampler. The delay line delays the IF signal that is used to sample the IF signal via DFFs. The DFF outputs, Q[63:0], generate a thermometer code depending on the frequency of IF. An encoder converts the thermometer code to a 6b binary code, S_{Period}, for the succeeding digital signal processing circuits. To reduce the hardware, the delay line consists of coarse and fine delay cells whose delay are ΔT_1(=180ns) and ΔT_2(=1ns), respectively. By choosing a 64-stage delay line, the demodulator can achieve ±350kHz frequency offset tolerance. The frequency offset tolerance could be extended by increasing the length of the delay line and the wordlength of the encoder.

The proposed TDC needs no closed-loop operation and can provide comparable performance with less hardware compared to the DLL-based TDC in [6] with the same dynamic range. An on-chip calibration circuit is also employed to minimize the delay changes due to temperature and supply voltage variation. Hence, with a decent length of the delay line, the demodulator can cover large frequency offset and drift. The performance of the GFSK demodulator, such as frequency offset tolerance and required SNR, is highly influenced by the accuracy of the delay line. To minimize delay variation caused by the noise from power supply, ground, and substrate, the delay cell is a differential circuit. Shown in Fig. 4.6.3, the differential delay cells are biased by a tunable current mirror. When the GFSK demodulator is turned on, it first performs the calibration. The calibration control logic sends a 5MHz reference signal to the delay line and an initial value to the tunable bias. The calibration circuit tunes the bias current of the delay line so that the encoded output is around the middle of the full scale. Therefore, the proposed delay line can provide accurate delay with low power and compact structure. With the delay-line calibration scheme, the GFSK demodulator can achieve consistent performance over –40°C to 85°C.

The GFSK demodulator is designed to support 1Mb/s and 250kb/s data rate. The limiter and regulator are included on chip for test considerations. A 5MHz Bluetooth-like modulated IF signal with 160kHz frequency deviation and additive white Gaussian noise (AWGN) is applied to the chip. Figure 4.6.4 shows the measured BER versus SNR. The demodulator requires SNR of 14.9dB to achieve 0.1% BER at 1Mb/s. For 250kb/s, the required SNR is 7.4dB at 0.1% BER. The low required SNR of the demodulator could further enhance the sensitivity of the receiver.

Figure 4.6.5 shows the required SNR versus input frequency offset. It indicates that the maximum frequency offset tolerance is ±350kHz. The co-channel rejection is also measured by adding another GFSK modulated signal at the same frequency as part of the input. For 0.1% BER, the demodulator achieves 9.5dB co-channel rejection. Figure 4.6.6 summarizes the performance of this delay-line-based GFSK demodulator.

Figure 4.6.7 shows the micrograph of the GFSK demodulator. The active area of the GFSK demodulator is 0.26mm^2. It is fabricated in a 0.18μm 1P4M CMOS technology and draws 2mA from a 1.8V supply.

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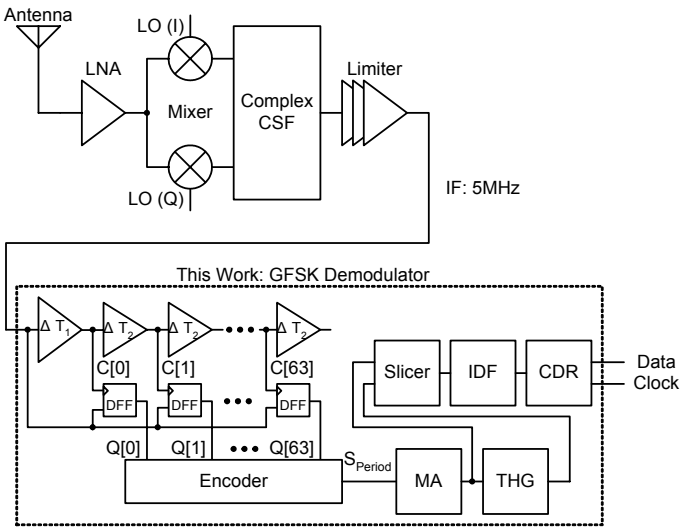

Figure 4.6.1: Block diagram of a low-IF receiver with the proposed GFSK demodulator.

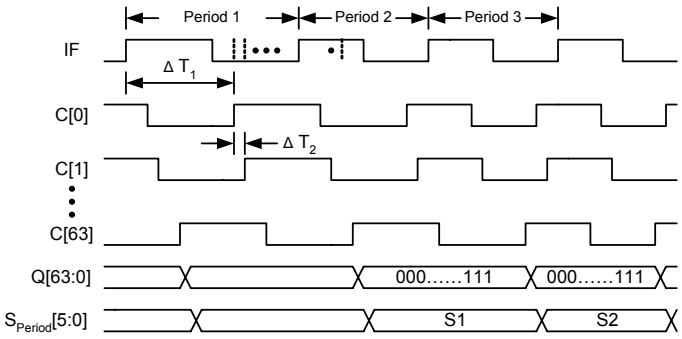

Figure 4.6.2: Principle of the proposed GFSK demodulator.

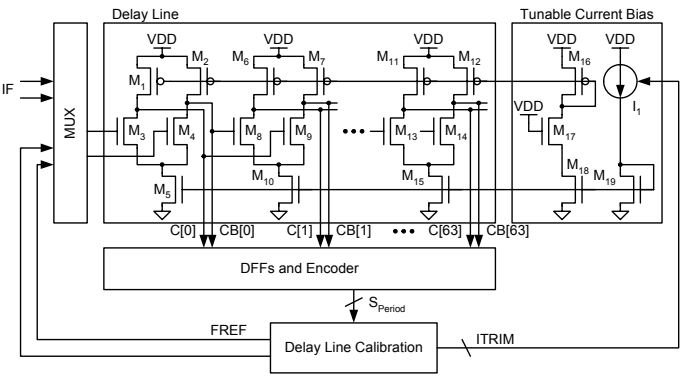

Figure 4.6.3: Self-calibrated delay line.

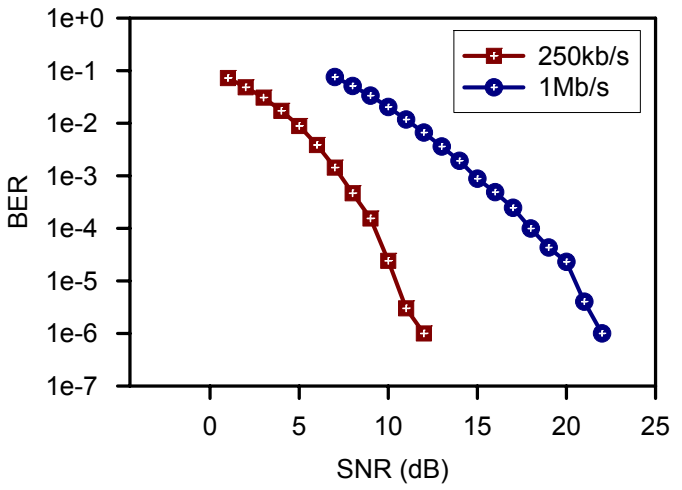

Figure 4.6.4: BER versus SNR.

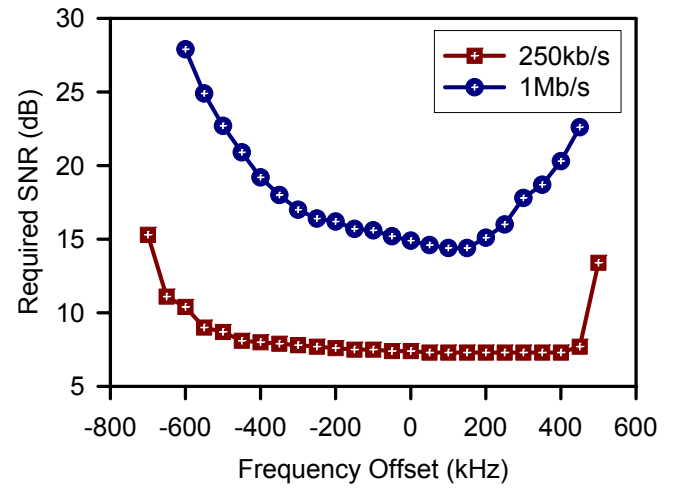

Figure 4.6.5: Required SNR versus frequency offset.

Technology	0.18μm 1P4M CMOS
Active Area	0.26mm^2
Current Consumption	2mA@1.8V
IF Frequency	5MHz
Modulation Format	GFSK (Bluetooth Format)
Data Rate	1Mb/s, 250kb/s
Required SNR (1Mb/s, 250kb/s)	14.9dB, 7.4dB
C/Ico-channel (1Mb/s, 250kb/s)	9.5dB, 4dB
Frequency Offset Tolerance (1Mb/s, 250kb/s)	±350kHz, -600kHz to 450kHz
Temperature Range	-40°C to 85°C

Figure 4.6.6: Performance summary.

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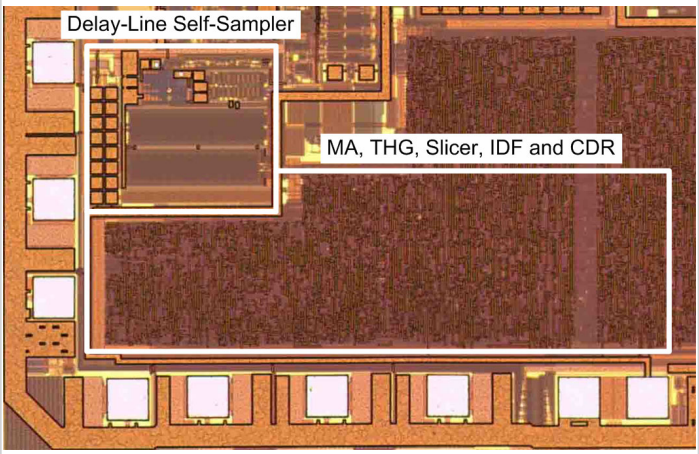

Figure 4.6.7: Chip micrograph.

